METHOD FOR CONVERTING A PLANAR TRANSISTOR DESIGN TO A VERTICAL DOUBLE GATE TRANSISTOR DESIGN

5 ## ABSTRACT

A method for creating a vertical double-gate transistor design includes providing a planar transistor layout (10) having a gate layer (12) overlying an active layer (14). In one embodiment, a first intermediate layer (18) is defined

10 based on an overlapping region of the gate and active layers, and, using the first intermediate layer, a second intermediate layer (22) is defined which defines a spacing between at least two fins of the vertical double-gate transistor design. The second intermediate layer may also define a length and a width of the at least two fins. One embodiment modifies a dimension of the first intermediate

15 layer prior to defining the second intermediate layer. The method further includes defining a resulting layer (24) based on a non-overlapping region of the second intermediate layer and the active layer. The resulting layer may then be used to create a mask and a semiconductor device (30) corresponding to the vertical double-gate transistor design.

20